SEMICONDUCTOR BUFFER STRUCTURES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the formation of strained semiconductor layers in the field of semiconductor manufacturing, and relates specifically to the formation of strained silicon on silicon germanium buffer layers.

2. Description of the Related Art

Strained semiconductor materials advantageously provide improved electrical carrier mobility properties as compared to relaxed semiconductor materials, thus increasing the speed at which semiconductor circuits can operate. A semiconductor layer is said to be "strained" when it is constrained to have a lattice structure in at least two dimensions that is the same as that of the underlying single crystal substrate, but different from its inherent lattice constant. Lattice strain occurs because the atoms in the deposited film depart from the positions normally occupied when the material is deposited over an underlying structure having a matching lattice structure. The degree of strain is related to several factors, including the thickness of the deposited layer and the degree of lattice mismatch between the deposited material and the underlying structure.

Strained semiconductor layers can be formed by epitaxially depositing silicon over a silicon germanium buffer layer. Silicon germanium films are used in a wide variety of semiconductor applications, such as in microelectronics fabrication. Because SiGe has a larger lattice constant than silicon, when epitaxial SiGe deposition occurs over silicon (such as during deposition on a silicon wafer), the epitaxially deposited SiGe is "strained" to the smaller underlying silicon lattice. If a strained silicon layer is to be deposited over the SiGe layer, the SiGe buffer layer should first be "relaxed" so that the silicon layer deposited thereover will be strained. In particular, because a strained SiGe layer has the dimensions of the underlying silicon lattice, a silicon layer deposited over a strained SiGe layer will not be strained. In contrast, a silicon layer deposited over a "relaxed" SiGe layer will be strained to conform to the larger underlying SiGe lattice. Thus, a strained silicon layer can be produced by epitaxially depositing silicon over a relaxed SiGe layer.

There are a number of approaches to forming a relaxed SiGe layer over silicon. In one approach, a SiGe layer is deposited beyond the "critical thickness." As the thickness of a strained SiGe layer increases beyond a certain "critical thickness", defects in the crystal structure of the strained SiGe layer appear, thereby inducing relaxation. After relaxation occurs, the degree of strain present in the SiGe layer is related to the amount of misfit dislocation generated in the layer during relaxation, which is a function of the elastic energy of the layer and the activation energy for dislocation nucleation and gliding. The critical thickness depends on a variety of factors, including growth rates, growth temperature, germanium concentration, and the number of defects within the layer underlying the SiGe layer.

In another approach, a graded SiGe buffer layer is deposited, with an increasing concentration of Ge from the underlying Si to the top surface. Unfortunately, when a thick graded buffer ("TGB") structure is grown, relaxation is often accompanied by vertically propagating threading dislocations and misfit dislocations. This occurs as a result of the lattice mismatch between the silicon substrate and the SiGe. Threading dislocations that are formed in the buffer layer propagate up into the overlying layer of strained semiconductor material, typically strained silicon, which can adversely affect device operation. Additionally, the surface of the graded buffer structure roughens as a function of the composition, leading to very high RMS surface roughness values.

By using various techniques during grading of the TGB structure, these deleterious effects can be reduced. For example, it has been shown that a linear change in germanium concentration at a grade rate of about 10% per micron produces a reduced defect level. While this method may be an improvement, the layers still suffer from a large number of threading dislocations and pile ups (a conglomeration of threading dislocations). Defect density for this method has been reported to be in the range of about $10^5/cm^2$ for threading dislocations and pile up counts in excess of 20/cm (Fitzgerald et al. Applied Physics Lett. 69 (7) 811, 1991). In addition, the layers still have a high roughness. Other examples of methods that have been tried to reduce defects include the use of strained super lattice structures to pin the threading dislocations (Obata et al. J. Appl. Phys. 81,199 (1997)) and the insertion of constant composition layers to pin threading dislocations at the interface.

SUMMARY OF THE INVENTION

In one aspect, the present invention relates to methods of forming a SiGe layer over a semiconductor substrate by a vapor deposition process, preferably a chemical vapor deposition (CVD) process, using vapor phase silicon and germanium precursors. Defects in the buffer layer are reduced by interrupting the flow of the silicon precursor at one or more intervals during deposition.

In some embodiments, a silicon precursor and a germanium precursor are flowed into a reaction space to deposit SiGe on a substrate in a first SiGe deposition phase. The flow of the silicon precursor into the reaction chamber is interrupted in a first interruption phase, while the germanium precursor continues to flow. The interruption phase preferably continues for less than about 10 seconds, more preferably less than about 5 seconds, after which the flow of the silicon precursor is resumed in a second SiGe deposition phase. The interruption phase results in the formation of an interface layer in the SiGe layer. Preferably the interface has a thickness of less than about 100 Å, more preferably less than about 50 Å and has a composition that differs from the overlying and underlying SiGe layer. In some embodiments two or more interruption phases are provided in the course of depositing the SiGe buffer layer. In some embodiments the SiGe deposited during the first and/or second SiGe deposition phases comprises an increasing concentration of germanium.

In another aspect of the invention, methods are provided in which a SiGe buffer layer with reduced defects is deposited on a substrate by continuously flowing a germanium precursor to a reaction chamber containing the substrate and intermittently flowing a silicon precursor to the reaction chamber. In some embodiments, the SiGe buffer layer preferably comprises an increasing concentration of germanium from an interface with the substrate to an interface with an overlying layer, such as a strained silicon layer.

In a further aspect, methods of forming a strained silicon layer on a substrate are provided. A SiGe buffer layer is preferably deposited on a substrate by a CVD process and a layer of strained silicon is deposited over the buffer layer. The CVD process preferably comprises at least one SiGe deposition phase, in which the substrate is contacted with a vapor phase silicon compound and a vapor phase germanium compound to deposit SiGe with an increasing Ge concentration, and at least one interruption phase, in which the substrate is contacted with a vapor phase germanium compound but not a